DEPARTMENT OF ELECTRONICS
COCHIN UNIVERSITY OF SCIENCE & TECHNOLOGY
KOCHI-682 022, INDIA

Report on 8th International Symposium on Embedded computing & System Design (ISED 2018)

The 8th International Symposium on Embedded computing & System Design (ISED 2018) was organised during 13-15th December 2018 in co-sponsorship with KSCSTE and CSIR. The programme was inaugurated by Sri. Mohammed Hanish IAS, MD of Kochi Metro Rail Limited on 13th December 2018 at Seminar Complex 2018 with the inaugural ceremony at 10 am. The registration for ISED 2018 started at 9.00 am in the Seminar complex, CUSAT. An Intelligent Embedded Systems Challenge (IESC) and A three-day workshop/FDP on Machine Learning was also organised as a part of ISED 2018.

Fig 1: Inauguration of ISED, IESC and ML Workshop by Shri. A. P. M. Mohammed Hanish IAS, Managing   Director KMRL

Professor Dr. Supriya M.H., of the Department of Electronics, extended the welcome speech to the dignitaries and delegates of ISED 2018. It was followed by the speech of Program chair of ISED 2018, Dr. Bijoy A. Jose on the 8th International Symposium on Embedded computing & system Design and it's relevance. The Honorable Vice Chancellor of Cochin University of Science & Technology Dr. R Sasidharan presided over the function. The Proceedings of ISED 2018 was released by Prof. Sandeep Shukla, General chair, ISED 2018 and Head of Computer Science and Engineering Department, Indian Institute of Technology, Kanpur, India and spoken about the successful organisation of ISED 2018. Words of felicitation were spoken by

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Prof. Gerhard W. Dueck, Professor of Computer Science, University of New Brunswick. The inaugural session was concluded by Vote of Thanks by Dr. Tripti S Warrior. Assistant Professor, Department of Electronics, CUSAT. It was followed by a morning tea break.

Fig 2: Proceedings release of ISED by Prof. Sandeep Shukla, Head of Computer Science and Engineering   Department, Indian Institute of Technology, Kanpur

After the tea break a Keynote Address on the topic "Cyber-Physical System Security: Convergence of Electrical Engineering and Computer Science" by Prof. Sandeep K. Shukla, Indian Institute of Technology, Kanpur. He talked about the cyber attacks and the need for improving security in our fast growing world. It was followed by an interactive session with Prof. Sandeep K. Shukla and many delegates utilised the opportunity to understand more about cybersecurity concerns. After the keynote, a technical session on Machine learning was conducted in the Seminar Hall with Dr. G. Santhosh Kumar, Head of the Computer Science Department, CUSAT and the presentation of Embedded Challenge in Industry category was organised at Executive Hall with Dr. Supriya M. H. as session Chair. Four papers were presented in the technical session and a presentation on "Basic Utility Lower Exoskeleton" from Astrex Innovations, Cochin was presented. At 1.00 pm the sessions were paused for a lunch break.

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Fig 3: Keynote address by Prof. Sandeep Shukla, Head of Computer Science and Engineering Department,   Indian Institute of Technology, Kanpur

After the lunch break at 2.00 pm the second keynote address by Mr. Arvind Raju, Senior Architect, Intel Corporation, India on the topic "Scalable and secure deployment of IoT devices". He explained about the different projects and development process happening in his company. After the keynote address the event was again divided for technical session on Machine learning was conducted in the Seminar Hall with Session Chair as Dr. B. Kannan, Head of the department, Department of Computer Application, CUSAT and the presentation of Embedded Challenge in Academic category was organised at Executive Hall with Dr. Tripthi S. Warrier as session Chair. Four papers were presented in the technical session and a presentation of various institutions was delivered. At 4.00 pm the sessions were paused for the evening tea break.

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Fig 4: Keynote by Mr. Arvind Raju, Senior Architect, Intel Corporation, India and Prof. Gerhard W. Dueck,

University of New Brunswick, Canada

Fig 5: Demo presentations by participants of IESC

After the tea break the third keynote on "Prospects and Challenges of Reversible Computing" by Prof. Gerhard W. Dueck, University of New Brunswick, Canada was arranged. The speaker talked about the research ongoing in his university and country. After the completion of keynote the programme was again divided for a technical session. In Seminar Hall technical session on VLSI System with Session Chair as Dr. Babita Roslind Jose, Associate Professor, Department of Electronics and Communication, SOE, CUSAT and Dr. P Mythili, Professor at School of Engineering CUSAT was the session chair for the technical session on Signal Processing. Four papers were presented in each technical session. At 6.30 pm the first day sessions were concluded and a Conference banquet was organised at RECCA club, Co-located with NITCAA and Kerala Start-up Mission.

On the second day of the conference, 14th December 2018 (Friday) the programme started at sharp 9.00 am with two parallel technical sessions in Seminar hall and Executive hall, and Machine learning workshop at Department of Electronics Auditorium. In Seminar Hall technical session on Communication Systems with Session Chair as Dr. Debesh Das, Professor Computer Science and

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Engineering Department Jadavpur University and in Executive hall, the session on Power-Aware Systems with Dr. S Mridula, Professor Division of Electronics Engg., School of Engineering, CUSAT as session chair. Three communication and four papers on signal processing were presented respectively in the sessions.

The tea break followed by technical session the Fourth keynote address was delivered by Dr. V.
Ramakrishna, Researcher, IBM Research India on the topic "Revamping Industrial Processes with Block chain". He explained in detail about the block chain management and the process flow and control as well the role of IBM in the field of block chain management.

Fig 4: Keynote by Dr. V. Ramakrishna, Researcher, IBM Research India and Dr. Shinya Honda, Associate   Professor, Graduate School of Informatics, Nagoya University

After the keynote address, the crowd was again divided for technical paper presentations. Papers on System Design and Security with session chairs Dr. Jimson Mathew, Associate Professor, IIT Patna & Dr. Shahana T K, Professor Division of Electronics Engg., School of Engineering was in seminar hall and papers on Embedded System Design with session chairs Dr. Philip Samuel, Professor, Department of Computer Science, CUSAT and Dr. James Kurian, Professor, Department of Electronics ,in executive hall was organised. Eight papers on respective topics were presented in the sessions. At 1.00 pm the sessions were paused for lunch break.

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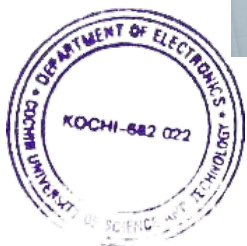**supriya@cusat.ac.in**
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After the lunch break at 2.00 pm the Fifth keynote address on "System Level Design Tool Set and RTOS for SoC FPGA" by Dr. Shinya Honda, Associate Professor, Graduate School of Informatics, Nagoya University. In his talk, he talked about the RTOS design tools and its importance in chip level designing was explained. It was followed by the sixth keynote address by

Dr. Lenin Gopal, Associate Professor, Curtin University, Miri, Malaysia on "IoT and Embedded systems" He explained in detail about embedded technology trends and its research scopes. At 3.15 pm the sessions were paused for an evening tea break.

After the tea break, the last technical session track on Signal Processing and VLSI System was organised in 2 venues with session chair Dr. Deepa Sankar, Associate Professor Division of Electronics Engg., School of Engineering and Dr. Nalesh S., Assistant Professor, Department of Electronics, CUSAT. Four papers were presented in each session. A valedictory function was organised at 4.45 pm in the seminar hall for the technical session. The Program Chair of ISED 2018 Dr. Bijoy A. Jose addressed and thanked the gathering for the smooth conduct of ISED 2018. Certificates for best paper presentations was awarded to Sree Ranjani R from Amrita School of

Engineering, Coimbatore, India on the paper "A Novel Logical Locking Technique against Keyguessing Attacks" and Purvi Patel from DA-IICT, Gandhinagar, India on the paper Low Power Management Unit with Load Regulation using DC-DC Switched Capacitor Converters in 0.18um CMOS. The programme was concluded at 5.15 pm.

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Fig 4: Delegates presenting their research papers in technical sessions

Report on Intelligent Embedded Systems Challenge (IESC)

An "Intelligent Embedded Systems Challenge (IESC)" was organised as a co-located event of the 8th International Symposium on Embedded computing & System Design (ISED 2018) in December 2018. This exciting competition for both academia and industry IESC was launched on 1st November 2018 to encourage innovative ideas from the participants. Identifying ideas in Intelligent, Embedded and Software/App controlled systems that can help people and society was the aim of this challenge.

Initially, the registered teams were requested to submit an abstract and report with its implementation, applications and future scope. We obtained an overwhelming response of more than 40 submissions from various academic institutions in the southern part of India. We had to stop accepting responses since giving a presentation opportunity to more than 40 applicants within a span of 10 days would be a challenge by itself. From these submissions, 30 teams were shortlisted to the next phase in which we conducted 15 minutes Skype interview with the team members.

Over a period of two weeks, a two-member panel had an interactive discussion with all the selected teams through Skype. Most of the teams were prepared for a demonstration of their project proposals that helped us to understand their status. The coordinators were Dr. Tripti Warrier of DOE CUSAT and Thomas Sabu of IEEE. Based on the Skype evaluation, six teams were shortlisted for the final presentation and demonstration on 13th December 2018 at the

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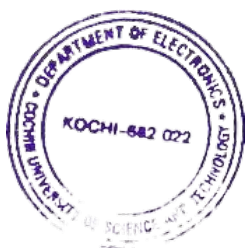**supriya@cusat.ac.in**
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prestigious ISED 2018 held at Cochin University of Science and Technology, Kerala. The List of the teams shortlisted for the academic track are:

1. Zone Adaptive Response System from Muthoot Institute of Technology and Science, Varikoli, Kerala.
2. Smart Transport Supervise System from KLE TECHNOLOGICAL UNIVERSITY, Hubli, Karnataka.
3. Web-Based Automated Farm Irrigation Control System using IoT from Multimedia University, Malaysia.
4. Real Time Garbage Monitoring Network form Department of Electronics, CUSAT, Kerala.
5. "I See It All" Implementation of Face Recognition Surveillance System Using FaceNet and MTCNN on Jetson TX2 from Department of Electronics, CUSAT, Kerala.
6. Driver Assistance Device from KLE TECHNOLOGICAL UNIVERSITY, Hubli, Karnataka.

Finals

Four out of the six teams shortlisted had demonstration booths at the ISED venue which got a lot of attention from students and professionals. The last level evaluation consisted of a threemember team from industry and academia. They were Sri Arvind Raju of Intel Corporation, Dr. Babita Jose of SOE, CUSAT and Dr. Deepti Das of DOE, CUSAT. The session was chaired by Dr. Supriya M H and Dr. Tripti Warrier of DOE, CUSAT. The evaluation was based on various demonstration and presentation on 13th December'18. The teams were judged based on criteria such as innovation, implementation and toughness of the project proposal. Judge interacting with participants of the embedded challenge during demonstration session ISED participants discussing with IESC finalists on their project winners and prize distribution.

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Fig 5: Judge interacting with participants of the embedded challenge during the demonstration session

Fig 6: ISED participants discussing with IESC finalists on their project

Winners and prize distribution.

The team with the project proposal titled "Driver Assistance Device" from KLE TECHNOLOGICAL UNIVERSITY, Hubli, Karnataka was chosen as the winner of IESC academic track. The prize money of Rs 25,000 sponsored by IEEE Circuits and Systems society

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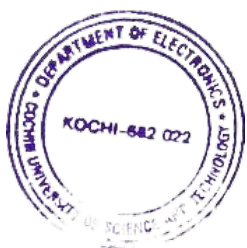supriya@cusat.ac.in
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was given to winners by Mr. Shilen Sagunan, organizer of the evening entrepreneurship event by Kerala Startup mission.

The industry track was won by "Basic Utility Lower Exoskeleton" from Astrex Innovations, Cochin.

The result of the challenge was announced and the prizes were distributed at the banquet dinner organised on the same day at NITCA club. Winners of IESC academic track being presented a memento by organizers.

Fig 7: Winners of IESC academic track being presented a memento by organizers

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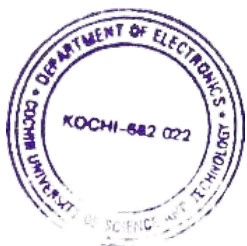### Report on Three-day workshop on "Machine Learning"

 A three-day workshop on "Machine Learning" was conducted at Department of Electronics, Cochin University of Science and Technology in colocation with the 8th International Symposium on Embedded Computing and System Design, (ISED 2018) from December 13-15, 2018. The Workshop/FDP was organized by Department of Electronics, Cochin University of Science and Technology and Amazon Corporation in association with IEEE ComSoc Kerala chapter. The workshop was coordinated by Mr. Arun A. Balakrishnan and Mr. Midhun Haridas T. P. Assistant

Professors of the Department of Electronics and Dr. Bijoy A. Jose, Programme chair of ISED 2018

 A total of 62 participants from all over India has registered and attended the workshop of which 24 participants were from the host institution CUSAT and the rest from other institutions. On 13th December 2018, the ISED 2018 included the paper presentations on Machine learning track. All the participants attended the Technical Session on Machine Learning and got a brief idea on current areas of research in the field of machine learning. 8 papers were presented during the technical session and different academicians from institutes like IITs, NITs and different Central and State Universities presented their papers on Machine learning.

A familiarisation workshop on machine learning basics was co-ordinated for three days. On 13th December 2018, software installation session was coordinated where the participants were directed to install necessary software required for the Machine Learning Workshop in their Laptop. Printed notes and booklets were distributed to the attendees.

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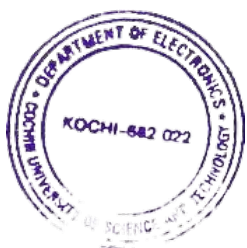## COCHIN UNIVERSITY OF SCIENCE & TECHNOLOGY
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Fig 8: Schedule of the Event at Department TV Screen

On 14th December the first session was familiarization of Amazon Web Services (AWS) by Mr. Sriram Kuravi, Solutions Architect-Cloud & IoT. He explained all the services provided over Amazon Web Services and how to do projects over them. The participants got the insight of the real-time applications like Cloud Computing services over AWS like Amazon Sagemaker Ground Truth, Amazon Recognition, Amazon Comprehend, Amazon Comprehend, Amazon Polly, Amazon Lex, Amazon Transcribe and Amazon Translate. After the tea break, the next session directed by Mr. Sachin Rout, Research Associate from Amazon was an introduction for Artificial Learning, Machine Learning and Deep Learning. It was a very informative session and we learned regarding the various parameters in Machine Learning and the difference between Deep Learning and Machine Learning. He had explained the difference between Deep Learning and Machine Learning and various architectures. Many real-time applications were including and the collaboration of AI, Machine Learning with the Internet of Things (IoT) was discussed. It was followed by a detailed explanation of Artificial Neural Network and the architecture of the same.

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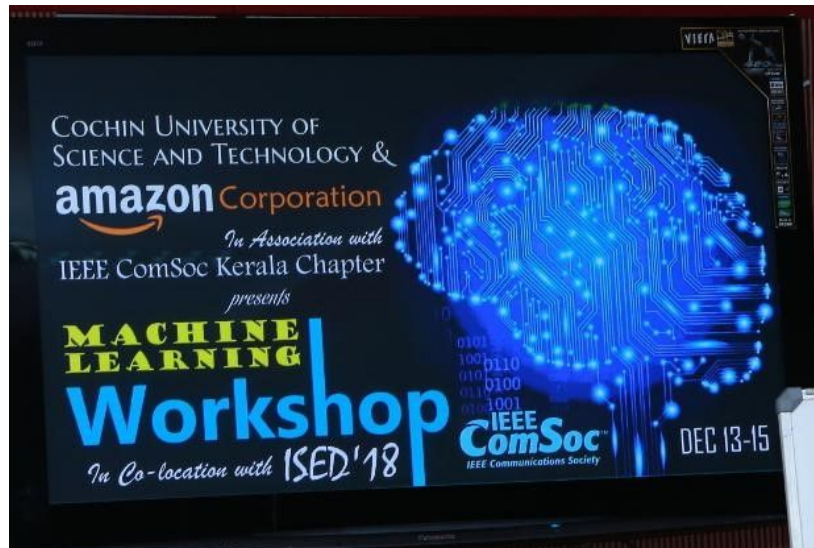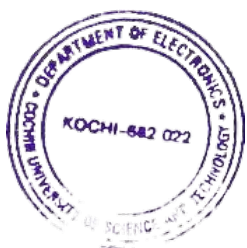supriya@cusat.ac.in
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Fig 9: Workshop Poster On TV Screen

The session was followed by trainer Mr. Arzan Amaria, Sr. Solutions Architect-cloud & IoT, he had explained the mathematical approach of an Artificial Neural Network and the mathematics and statistics behind it. It was followed by lunch and in the post-lunch session again Mr. Sachin Rout, Research Associate, has taken the session on Deep Learning and Shallow Learning. It was followed by a hands-on session where all the participants actively participated and the basic code for prediction and classification problem was carried on. We were explained about various platforms for Machine Learning applications. Later we had QA sessions and it was a very informative and interactive session. Later the dignitaries were honoured with the memento and the program was concluded by 5 pm.

On the next day on 15th October, we had the first introduction of perceptron and Artificial Neural Network by Mithun Sir, Assitant Professor, Department of Electronics, CUSAT. He had explained the similarity of a biological neuron and Artificial Neuron, a perceptron. He had explained about working of a perceptron and different types of Neural Network. It was followed by a tea break and post tea break the session was directed by Dilip Thomas.

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Fig 10: Workshop at Department of Electronics Auditorium

He directed a very interactive session on Computer Vision and Deep Learning. He had explained about various real-time applications of Computer Vision using Deep Learning like realtime object detection, Image segmentation, a decision based on the classification of the image. He had shown the implementation of Deep Learning in the Computer Vision and the applications. He later explained the basics of Convolutional Neural Network (CNN) and its working.

He explained the various operations involved in a Convolutional Neural Network like convolution, pooling, noisy image data cancellation, striding. It was an informative session and the It was followed by lunch and in the post-lunch session, we had a hands-on session were sir had explained the working of the code of a binary image classification problem. He had explained the challenges in real-time applications and how to solve them. It was a detail explanation of how CNN performs a basic image classification. It was an interactive session and all the participants actively participated.

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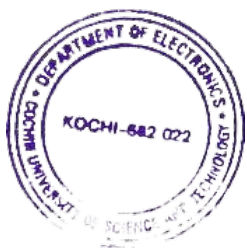**supriya@cusat.ac.in**
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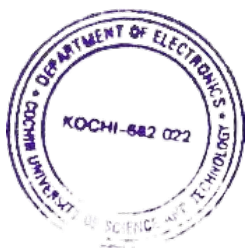
Fig 11: Workshop Session by Mr Dilip Thomas at Department of Electronics Auditorium

The program was concluded by 4.30 with the Certificate distribution and Dilip Thomas was honoured with a memento by Dr. Bijoy A. Jose

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Fig 12: Workshop participants at Department of Electronics Auditorium

Participant List of ISED 2018

SI No	Name of the Keynote speaker/ Participant	Designation	Institute/College/ University	Email	Speaker/Title of the Paper
	International Keynote speakers				
1	Shinya Honda	Professor	Nagoya University	honda@ertl.jp	Keynote Speaker
2	Gerhard Dueck	Professor	University of New Brunswick, Canada	gdueck@unb.ca	Keynote speaker
3	Lenin Gopal	Professor	Curtin University, Miri, Malaysia	lenin@curtin.edu.my	Keynote Speaker
	International Delegates				
4	Masataka Ogawa	Student	Nagoya University	masa-bach@ertl.jp	Efficient Approach to Ensure Temporal Determinism in Automotive Control Systems
5	Anu Bala	Student	Oxford Brookes University, Oxford, UK	15057719@brookes.ac.uk	A Memristive Activation Circuit for Deep Learning Neural Networks
	National Delegates				
6	Anirban Ganguly	Student	Indian Institute of Engineering Science and Technology Shibpur	gangulyanirban8@gmail.com	A Highly Accurate Current Mode Analog Implementation of Radix-2 FFT/IFFT Processor
7	Anagha V S	Student	COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY	anaghavspragathy@gmail.com	Channel and Doppler Estimation In Underwater Communication
8	Muhammed Anees V	Student	CUSAT	anees@cusat.ac.in	Deep Learning Framework for Density Estimation of Crowd Videos

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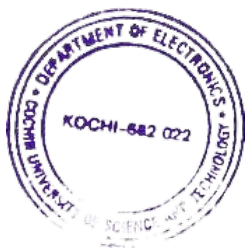**Head of the Department**
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9	Deepa Sankar	Faculty	Cochin University of Science and Technology	deepasankar@cusat.ac.in	Implementation of Compressive Sensing for Speech Signals
10	George Eldho John	Individual	College of Engineering Trivandrum	georgeeldhojohn@gmail.com	Application specific WSN for precision agriculture
11	Avishek Choudhury	Faculty	New Alipore College	avishek.nac.cs@gmail.com	ReMiT: Redundancy Migration for Latency Aware Fault Tolerant Cache Design in Multicore
12	Harikrishnan Venugopal	Faculty	Amrita Vishwa Vidyapeetham	harikrishnanv@am.amrita.edu	Design of a Low-cost Universal Colour Sensor to Support Rural Healthcare
13	Ahmed Shaban	Student	ALIGARH MUSLIM UNIVERSITY	ahmedshaban@zhcet.ac.in	Compact and Reliable Low Power Non-Volatile TCAM Cell
14	Madhuri Panwar	Student	IIT Hyderabad	ee15resch01004@iith.ac.in	Non-invasive Blood Glucose Estimation Methodology Using Predictive Glucose Homeostasis Models

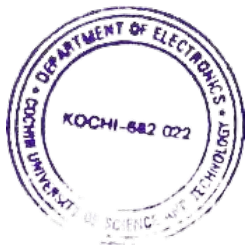| 15	Sumit Kumar	Student	IIT Patna	sumitphd13@gmail.com	A Robots Sharing Based Encryption Method in Singular Value Decomposition Domain Using Fractional Fourier Transform
16	Sriram Sankaran	Faculty	Amrita Vishwa Vidyapeetham	srirams@am.amrita.edu	Game Theoretic Modeling of Power-Performance Trade-offs for Mobile Devices
17	Lokesh Jigalur	Student	DA-IICT, Gandhnagar	201611029@daiict.ac.in	An Iterative Delay Chain based Impedance to Digital Converter in 0.18um CMOS
18	Yash A Vora	Student	DA-IICT	vorayash13@gmail.com	A Wearable Device for Real-Time ECG Monitoring and Cardiovascular Arrhythmia Detection for Resource Constrained Regions
19	Suvadip Hazra	Student	NIT DURGAPUR	suvadip.093016@gmail.com	Evaluation and Detection of Hardware Trojan for Real-Time Many-Core Systems

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20	George Eldho John	Individual	College of Engineering Trivandrum	georgeeldhojohn@gmail.com	Application specific WSN for precision agriculture
21	Piyoosh Purushothaman Nair	Student	Indian Institute of Technology Guwahati	piyoosh@iitg.ac.in	FEST: Fault-Tolerant EnergyAware Scheduling on Two-Core Heterogeneous Platform
22	Abhishek Singh	Faculty	Jadavpur University	drkisku@gmail.com	Detection of Rare Genetic Diseases using Facial 2D Images with Transfer Learning
23	Kala S	Ph. D Scholar	SOE, CUSAT	kalas19@gmail.com	Design Space Exploration of Convolution Algorithms to Accelerate CNNs on FPGA
24	Nilanjana Das	Student	Indian Institute of Engineering Science and Technology, Shibpur	dasnilanjana286@gmail.com	Hard to Detect Combinational Hardware Trojans
25	Vimala Mathew	Student	NIELIT Calicut	vimalamathew@gmail.com	Prediction of suitable human resource for replacement in skilled job positions using Supervised Machine Learning.
26	Shimmi Asokan	Ph. D Scholar	CUSAT/RSET	shimmi_a@rajagiritech.edu.in	Modelling and Verification of the FlexRay Startup Mechanism Using UPPAAL Model Checker
27	Michael George	Student	CUSAT	michaelgeorge2010@gmail.com	Crowd Panic Detection Using Autoencoder with Non-uniform Feature Extraction
28	Chinnaiah M C	Faculty	B V Raju Institute of Technology	chinnaaiah.mc@bvrit.ac.in	A New Deliberation of Embedded based Assistive System for Yoga
29	Mini P P	Student	Department of electronics, CUSAT	minidevutty@gmail.com	Feature Vector Selection of Fusion of MFCC and SMRT Coefficients for SVM Classifier Based Speech Recognition System

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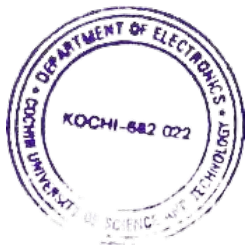| 30	Biswajit bhowmik	Faculty	IIITDM Kurnool	brb@iiitk.ac.in	A Time-Optimized Test-Solution Scheme for the Analysis of Permanent Faults on NoC Interconnects
31	Purvi Patel	Student	Dhirubhai Ambani Institute of Information and Communication Technology	201521008@daiict.ac.in	Low Power Management Unit with Load Regulation using DCDC Switched Capacitor Converters in 0:18um CMOS
32	Rose George Kunthara	Student	SCHOOL OF ENGINEERING, CUSAT	rosekunthara87@gmail.com	ReDC: Reduced Deflection CHIPPER Router for Bufferless NoCs
33	Dr Mini P R	Faculty	Federal Institute of Science and Technology	mini@fisat.ac.in	Performance Enhancement of Sample Matrix Inversion Beamformer Using A Novel Algorithm
34	Dr. Baisakhi Das	Faculty	Institute of Engineering and Management, Salt Lake, Kolkata	baisakhi.das@iemcal.com	Stuck-At 0/1 Trojans on Return Address Stack
35	N Shekar V Shet	Faculty	National Institute of Technology Karnataka, Surathkal	ash11etc@gmail.com, shekar_shet@yahoo.com	Challenges for Decentralized Congestion Control Mechanisms in Vehicular Ad Hoc Networks
36	Nripesh Kumar	Student	NIT Trichy	nripeshkmr88@gmail.com	Intelligent Intrusion Detection System using Decision Tree Classifier and Bootstrap Aggregation
37	Sangeetha G S	Working.	NITK Surathkal	sangeethagramas@gmail.com	Trace-Driven Simulation and Design Space Exploration of Network-on-Chip Topologies on FPGA
38	Anindan Mondal	Student	NIT Durgapur	anindanmondal14@gmail.com	XOR based Methodology to Detect Hardware Trojan utilizing the Transition Probability
39	Ujjwal pasupulety	Student	National Institute of Technology Karnataka, Surathkal	15it150.ujjwal@nitk.edu.in	Thermal Aware Design for Through-Silicon Via (TSV) based 3D Network-on-Chip (NoC) Architectures

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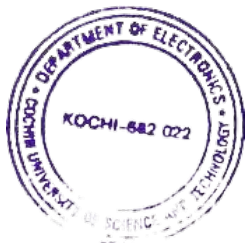
40	Phrangboklang Lyngton Thangkhiew	Student	National Institute of Technology Meghalaya	phrangboklang@nitm.ac.in	Fast In-Memory Computation of Boolean Functions in Memristive Crossbar Array
41	Dr. Ipsita Biswas Mahapatra	Faculty	Atria Institute of Technology	ipsita.mahapatra@gmail.com	An Algorithm - Architecture Co-Designed System for Dynamic Execution-Driven Pre-Silicon Verification
42	Khushboo Rani	Student	IIT GUWAHATI	khushboo@iitg.ac.in	Non-blocking Gated Buffers for Energy Efficient on-chip Interconnects in the era of Dark Silicon
43	Naveen Murali G	Student	Indian Institute of Technology Kharagpur	nvz.naveenmurali@gmail.com	MODELLING AND SIMULATION OF NON-IDEAL MAGIC NOR GATES ON MEMRISTOR CROSSBAR
45	Chirag Joshi	Student	College Of Engineering, Pune	chiragbjoshi2@gmail.com	Towards Analysing the Effect of Snoozy Caches on the Temperature of Tiled Chip Multi-Processors
46	Sree Ranjani R	Student	AMRITA VISHWA VIDYAPEETHAM	r_sreeranjani@cb.amrita.edu	A Novel Logical Locking Technique against key-guessing attacks
47	Mahabub Hasan Mahalat	Student	NIT Durgapur	mahabubhasan.mahalat@gmail.com	A PUF based Light Weight Protocol for Secure WiFi Authentication of IoT devices
48	Anirban Chakraborty	Student	IIEST, SHIBPUR	chakraborty.sab@gmail.com	Low Area & Memory Efficient VLSI Architecture Of 1D/2D DWT For Real Time Image Decomposition
49	Chinnaiah.M C	Faculty	B V Raju Institute of Technology	chinnaaiah.mc@bvrit.ac.in	Hardware Scheme for Autonomous Docking Algorithm using FPGA based Mobile Robot

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